Amendments to the Specification:

In paragraph [0008]:

It is therefore a primary objective of the claimed invention to provide a processing system having a bus controller, the processing system for ~~directly~~ updating firmware stored in a non-volatile memory without utilizing a processor to solve the above-mentioned problems.

In paragraph [0021]:

However, the major differences between the two processing systems 10 and 30 are that the processing system 10 utilizes the processor 16 to connect the NVM control interface 14 with the serial port interface 18 and to process the update data, while ~~and that~~ the serial port interface 38 of the processing system 30 is directly electrically connected to the NVM control interface 34. Additionally, the NVM control interface 34 is capable of using the data bytes that are generated by converting the serial bits received from the computer 40 to update the firmware stored in the NVM 32.

In paragraph [0024]:

Please refer to Fig. 4 that is a functional block diagram of the NVM control interface 34. The NVM control interface 34 comprises an NVM address register 92 for ~~setting~~ specifying addresses of the NVM 92, an NVM page register 93 for ~~setting~~ specifying a download capacity of the NVM 32, an NVM data register 94 for storing a data byte stored in the address set by the NVM address register 92, a plurality of control bits 95 for ~~setting~~ specifying an operational mode of the NVM 32, and a plurality of command registers 96 for ~~executing~~ specifying commands to control operations of the NVM 32. Additionally, after each write/read (W/R)

operation of the NVM 32 is finished, the address stored in NVM address register 92 is ~~increased~~incremented. In the embodiment, a serial port 42 of the serial port interface 38 for connecting to the computer 40 is an RS-232 (Recommended Standard-232) port. For the purposes of this description, the processing system 30 will be used to identify a device as described above, but this should not construe the present invention as limited.

In paragraph [0041]:

During the initial period, the statuses of the registers, such as the NVM address register 92 and the NVM page register 93, of the NVM control interface 34 are reset. During the loading period, the write command and the update data are transmitted to the NVM control interface 34. Meanwhile, the NVM control interface 34 reads a ~~prior~~ previous piece of data that is stored in the NVM 32 prior to the current piece of data and transmits the previous~~prior~~ piece of data to the computer 40 for comparison. Then the NVM control interface 34 updates the current piece of data in the NVM 32 and the address stored in NVM address register 92 is increased. Moreover, the previous~~prior~~ piece of data may not be read and transmitted from the NVM 32 to the computer 40 for comparison until the update data for updating an entire page of the NVM 32 has been transmitted to the NVM control interface 34 so that switches in the data transmission direction between the processing system 30 and the computer 40 can be reduced. Finally, the update of the NVM 32 ends within the termination period.

In paragraph [0045]:

Step 65: receiving the update data from the computer 40 and reading a previous~~prior~~ piece of data that is stored in the NVM 32 prior to the current piece of data and transmitting the previous~~prior~~

piece of data to the computer 40 for comparison;

In paragraph [0050]:

After the NVM control interface 34 receives the write command, the NVM control interface 34 waits for the update data from the computer 40. When NVM control interface 34 receives the update data, NVM control interface 34 first reads the previous~~prior~~ piece of data from the NVM 32 and transmits the previous~~prior~~ piece of data to the computer 40 for comparison, and then the NVM control interface 34 writes the update data into the NVM 32 and the address stored in the NVM address register 92 is increased automatically. Finally, the processing system 30 finishes updating the firmware stored in the NVM 32.

In paragraph [0068]:

During the initial period, the statuses of the registers, such as the NVM address register 92 and the NVM page register 93, of the NVM control interface 34 are reset. During the loading period, the write command and the data for the update of the NVM 32 are transmitted to the NVM control interface 34. Meanwhile the NVM control interface 34 reads a previous~~prior~~ piece of data that is stored in the NVM 32 prior to the current piece of data and transmits the previous~~prior~~ piece of data to the computer 40 for comparison. If the previous~~prior~~ piece of data received from the NVM control interface 34 is not identical with the corresponding data recorded by the computer 40, the action for updating the firmware stored in the NVM 32 is terminated. Finally, the update of the NVM 32 ends within the termination period.